

ABSTRACT

A memory device is provided. The memory device comprises a substrate, first isolation structures, stacked device structures, and second isolation structures. The substrate comprises a memory cell area and a periphery area having trenches therein. Each stacked device structure is disposed between two neighboring trenches over the substrate. The stacked device structure comprises a gate dielectric layer and a gate layer. The gate dielectric layer covers part of the substrate. The second isolation structures are disposed between neighboring stacked device structures. The second isolation structure comprises a liner and an isolation layer. The liner is disposed on the sidewalls of the gate dielectric layer, the surface of the trenches, and the surface of the substrate not covered by the dielectric layer. The liner over the surface of the substrate not covered by the dielectric layer has a round curve. The isolation layer covers the liner, and fills the trenches.